Verichip: State Machine Test Plan

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1. Verichip in **Reset State** (Sections 6.1, 6.2, 6.5, 5.2).

   1.1 **Objective**:

   Verify that the state machine enters and remains in the Reset state whenever the active-low rst_b signal is asserted, regardless of other inputs. Additionally, verify that the state machine only transitions out of the Reset state to the Normal state when the specific input condition Maroon = 0, Gold = 1 is met while reset is inactive.

   1.2 **Plan**:

   Test all 16 possible combinations of the MGCE signals (Maroon, Gold, bad command, export violation) while rst_b is inactive (1) to ensure only the 01xx combinations trigger a transition. It will also include a test case where rst_b is active with don't care inputs to verify the reset behavior.

   1.3 **Test Table**:

Test Name	Signals (MGCE)	Reset (active low)	Next state	Test Description
SM_rst_0	0000	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] should display a value of 4'h0.
SM_rst_1	0001	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] should display a value of 4'h0.
SM_rst_2	0010	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] should display a value of 4'h0.
SM_rst_3	0011	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] should display a value of 4'h0.
SM_rst_4	0100	1	Normal	This will cause the state machine to transition to the normal state. The status register status_reg [3:0] should now show the value 4'h1.
SM_rst_5	0101	1	Normal	This will cause the state machine to transition to the normal state. The status register status_reg [3:0] should now show the value 4'h1.

SM_rst_6	0110	1	Normal	This will cause the state machine to transition to the normal state. The status register status_reg [3:0] should now show the value 4'h1.
SM_rst_7	0111	1	Normal	This will cause the state machine to transition to the normal state. The status register status_reg [3:0] should now show the value 4'h1.
SM_rst_8	1000	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_9	1001	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_10	1010	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_11	1011	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_12	1100	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_13	1101	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_14	1110	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_15	1111	1	Reset	Commands are disregarded during reset, resulting in the state machine staying in the reset state. The status register status_reg [3:0] is expected to display a value of 4'h0.
SM_rst_active	xxxx	0	Reset	When the system is in the reset state, activating the rst_b pin should ensure that the state machine remains in the reset state, regardless of any other input signals. The status register status_reg [3:0] should display a value of 4'h0.

1.4 **Footnotes**:

1.4.1 In the reset state, commands are ignored but all registers are accessible for reads and writes as specified.

1.4.2 The Status Register's "Operation Status" field should read 4'h0 while in this state.

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2. Verichip in **Normal State** (Sections 6.1, 6.2, 6.3, 6.4, 6.5, 5.2).

2.1 **Objective**:

Verify that the state machine remains in the Normal State (status_reg [3:0] = 4'h1) under valid conditions. Verify that an internally generated bad_cmd signal forces a transition to the Error state (status_reg [3:0] = 4'h2), and exp_vio forces a transition to the Export Violation state (status_reg [3:0] = 4'h8).

2.2 **Plan**:

Test all 16 combinations of the MGCE signals while in the Normal state to ensure proper exit paths. Export violation triggers when an unauthorized command is requested while export_disable is asserted. A bad command triggers when an undefined command is requested.

2.3 **Test Table:**

Test Name	Signals (MGCE)	Reset (active low)	Next state	Test Description
SM_norm_0	0000	1	Normal	This will result in the state machine staying in the normal state. The status register status_reg [3:0] should now display the value 4'h1.
SM_norm_1	0001	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status register status_reg [3:0] should display the value 4'h8.
SM_norm_2	0010	1	Error	This action should trigger the State Machine to enter the Error state. Additionally, the status

				register status_reg [3:0] should display the value 4'h2.
SM_norm_3	0011	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status register status_reg [3:0] should display the value 4'h8.
SM_norm_4	0100	1	Normal	This will result in the state machine staying in the normal state. The status register status_reg [3:0] should now display the value 4'h1.
SM_norm_5	0101	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status register status_reg [3:0] should display the value 4'h8.
SM_norm_6	0110	1	Error	This action should trigger the State Machine to enter the Error state. Additionally, the status register status_reg [3:0] should display the value 4'h2.
SM_norm_7	0111	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status register status_reg [3:0] should display the value 4'h8.
SM_norm_8	1000	1	Normal	This will result in the state machine staying in the normal state. The status register status_reg [3:0] should now display the value 4'h1.
SM_norm_9	1001	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status register status_reg [3:0] should display the value 4'h8.
SM_norm_10	1010	1	Error	This action should trigger the State Machine to enter the Error state. Additionally, the status register status_reg [3:0] should display the value 4'h2.
SM_norm_11	1011	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status

				register status_reg [3:0] should display the value 4'h8.
SM_norm_12	1100	1	Normal	This will result in the state machine staying in the normal state. The status register status_reg [3:0] should now display the value 4'h1.
SM_norm_13	1101	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status register status_reg [3:0] should display the value 4'h8.
SM_norm_14	1110	1	Error	This action should trigger the State Machine to enter the Error state. Additionally, the status register status_reg [3:0] should display the value 4'h2.
SM_norm_15	1111	1	Export Violation	This action should trigger the State Machine to move to the Export Violation state. Consequently, the status register status_reg [3:0] should display the value 4'h8.
SM_norm_rst	xxxx	0	Reset	When the system is in the normal state, activating the rst_b pin should make a transition in the state machine to the reset state, regardless of any other input signals. Additionally, the status register status_reg [3:0] should display a value of 4'h0.

2.4 **Footnotes:**

2.4.1 In this state, commands may be executed and all registers are accessible for reads and writes as specified.

2.4.2 The case where bad_cmd = 0 and exp_vio = 1 is technically undefined behavior. It is directed to Export Violation here for coverage mapping.

2.4.3 Status Register's "Operation Status" field should read 4'h1.

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3. Verichip in **Export Violation State** (Sections 6.1, 6.3, 6.5, 5.2).

3.1 **Objective**:

Verify that the state machine remains in the export violation state when triggered, with status_reg [3:0] holding 4'h8. Validate that all commands

(bad_cmd variations) are ignored in the export violation state. Verify that the only way out of the Export Violation state is a reset.

3.2 **Plan**:

Evaluate all 16 MGCE combinations to guarantee the state machine does not erroneously transition back to Normal or Error states. Assert rst_b to ensure the transition to Reset functions correctly.

3.3 **Test Table**:

Test Name	Signals (MGCE)	Reset (active low)	Next state	Test Description
SM_exp_0	0000	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_1	0001	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_2	0010	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_3	0011	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_4	0100	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_5	0101	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.

SM_exp_6	0110	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_7	0111	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_8	1000	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_9	1001	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_10	1010	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_11	1011	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_12	1100	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_13	1101	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_14	1110	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state,

				where the status register status_reg [3:0] should read 4'h8.
SM_exp_15	1111	1	Export Violation	Commands are disregarded during export violation state. This will result in the state machine staying in the export violation state, where the status register status_reg [3:0] should read 4'h8.
SM_exp_rst	xxxx	0	Reset	When the state machine is in the export violation state, asserting the rst_b pin should force a transition to the reset state, regardless of any other inputs. The status register status_reg [3:0] should then read 4'h0.

3.4 **Footnotes**:

3.4.1 In this state, commands are disabled and registers are reset except for the interrupts and interrupt enables.

3.4.2 Only the Chip Status Register may be read, all other reads and writes are disabled

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4. Verichip in **Error State** (Sections 6.1, 6.2, 6.4, 6.5, 5.2).

   4.1 **Objective**:

   Verify that the state machine remains in the error state when triggered, with status_reg [3:0] holding 4'h2. Validate that the state machine transitions to the normal state (status_reg [3:0] = 4'h1) under valid conditions (MG').

   4.2 **Plan**:

   Test all 16 MGCE combinations to ensure that only sequences where M=1 and G=0 allow an exit to the Normal state. Verify that asserting rst_b forces the state machine back to the Reset state.

   4.3 **Test Table**:

Test Name	Signals (MGCE)	Reset (active low)	Next state	Test Description
SM_err_0	0000	1	Error	Commands are disregarded in error state. This will result in the state machine

				staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_1	0001	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_2	0010	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_3	0011	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_4	0100	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_5	0101	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_6	0110	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_7	0111	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_8	1000	1	Normal	Commands are disregarded in error state. This will result in the state machine changing to normal state, where the status register status_reg [3:0] should read 4'h1.
SM_err_9	1001	1	Normal	Commands are disregarded in error state. This will result in the state machine changing to normal state, where the status register status_reg [3:0] should read 4'h1.
SM_err_10	1010	1	Normal	Commands are disregarded in error state. This will result in the state machine changing to normal state, where the status register status_reg [3:0] should read 4'h1.

SM_err_11	1011	1	Normal	Commands are disregarded in error state. This will result in the state machine changing to normal state, where the status register status_reg [3:0] should read 4'h1.
SM_err_12	1100	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_13	1101	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_14	1110	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_15	1111	1	Error	Commands are disregarded in error state. This will result in the state machine staying in the error state, where the status register status_reg [3:0] should read 4'h2.
SM_err_rst	xxxx	0	Reset	When the state machine is in the error state, asserting the rst_b pin should force a transition to the reset state, regardless of any other inputs. The status register status_reg [3:0] should then read 4'h0.

4.4 **Footnotes**:

4.4.1 In this state, commands are disabled, reads are enabled but writes are disabled.

4.4.2 The Status Register's Operation Status (status_reg [3:0]) field should read 4'h2 while in this state.

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